S

(b) Draw the block-diagram of 80186 up and explain its various features?

What is MDS? How can it be used in trouble shooting of up base system? Explain in details.

5. Write short notes on any three of the following

(a) RISC Processor

(b) Bit-Sliced processor

(c) Addressing Modes of 8086 up

(d) Segment and base registers of 8086 up

Discuss basic DMA operation with the help of suitable diagram.

(a) Explain cache structure of pentium.

(b) What is BIST and how is it activated?

8. How is the memory system of the pentium organised? Describe parity checking and generation indicating the signal pins.

What are the five groups of interrupts supported on 8086 CPU ?

*

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(4)

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2015

Time: 3 hours

Full Marks: 80

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Answer from both the Groups as directed.

Group - A

(Objective-type Questions)

Answer all questions.

1. Choose the correct answer of the following:

 $2 \times 10 = 20$

(a) The register that keeps the track of program during execution is:

(i) Address register

(ii) Data register

(iii) Program counter

(iv) Instruction register

ME - 19/1

(Turn over)

6 6	į. (a)	(f) How many I/O addresses can the 80 386 up		(i) 8-bit up (ii) 16-bit up (Long-	(e) The 8086 is a:	(iii) Execute-state (iv) Interrupt state (iii) 1 G	(i) Halt state (ii) Fetch-state (i) 1 M	to:	(d) The up after completing the execution returns (j) How man	(iii) Control-lines (iv) Input-liners (iii) 24-bit		memory on 32-number of: (i) The 808		(ii) Inpu	le (h)	(i) Clock-cycle (iii) 80386	information is:	(b) The cycle required to fetch and execute (g) Which u	
the maximum mode ?	Explain the PIN-discription of 8086 up for	ain the architecture	Answer any four questions of the following : $15 \times 4 = 60$	(Long-answer type Questions)	Group - B	1 GB (iv) 2-GB	1 MB (ii) 16 MB	80286 up Lave ?	How many physical memory locations can the	24-bit (iv) None of these	16-bit (ii) 20-bit	The 8086 up has the total address lines of	ectional	Inputs (ii) Outputs	The $A_0 - A_3$ address-lines of 8257 DMA controller are:	80386 (iv) None of these	8086 (ii) 80286	(g) Which up supports L-2 cache?	